WHITE PAPER

ESD Phenomena and the Reliability for Microelectronics

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White Paper

ESD Phenomena and the Reliability for Microelectronics

by the ESD Association

White Paper on Electrostatic Discharge (ESD) Phenomena

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Foreword

This white paper addresses the importance of ESD on Electronic Circuits. The objective is to present an insight into the present-day phenomena, an overview of its effects on electronic chips and systems, and a summary of the future issues and challenges facing ESD reliability as further advances in the semiconductor technologies are made.

With contributions from several leading experts in the different areas of the field, the state-of-the-art information about ESD is presented here in different chapters. These include details of controlling the ESD threat from the factory point of view to designing ESD on the IC chip itself. They also cover the methods to measure and test the ESD levels, the impact of the advanced IC technologies, simulation of the ESD effects, and finally the real challenges facing the ESD reliability for the next decade.

It is intended that this white paper will inform the reader about the serious nature of ESD for the next generation of electronics and subsequently the urgent need to make further research to maintain safe operation of these devices, whether they may be for consumer, industrial, military, or medical applications. It is further aimed that research organizations and government agencies will benefit from the contents of this document to allow for funding and encouragement of research and development in ESD.

The document assumes knowledge of the fundamentals of ESD, and the three main stress test models used for evaluating ESD on components: Human Body Model (HBM), Machine Model (MM) and the Charged Device Model (CDM). HBM and MM test for the transfer of charge to the Integrated Circuit (IC) pin, and CDM simulates the discharge from the IC package itself to a low impedance ground. For further information please refer to the documents at the ESD Association web site: www.esda.org.

Acknowledgments

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Chapter 1

The ESD Threat

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As we enter the next millennium, there are clear technological patterns. First, the electronic industry continues to scale microelectronic structures to achieve faster devices, new devices, or more per unit area. Secondly, electrostatic charge, electrostatic discharge (ESD), electrical overstress (EOS) and electromagnetic emissions (EMI) continue to be a threat to these scaled structures. This dichotomy presents a dilemma for the scaling of semiconductor technologies and a future threat to new technologies. Technological advancements, material changes, design techniques, and simulation can fend off this growing concern – but to maintain this ever-threatening challenge, one must continue to establish research and education in this issue. Research, development and education can help guide the path and direction such that the technological directions and ESD sensitivity of future devices are in harmony.

A detailed summary of the emerging technologies and their impact on ESD capability is given in Chapter 10.

Chapter 2

ESD Program Management

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INTRODUCTION

Electrostatic discharge (ESD) events can have serious detrimental effects on the manufacture and performance of microelectronic devices, the systems that contain them and the manufacturing facilities used to produce them. Submicron device technologies, high system operation speeds, and factory automation are making ESD control programs a critical element in the quality and reliability of ESD-sensitive (ESDS) products.

The detrimental effects that ESD has on sensitive electronic devices and assemblies are well documented and now receive considerable attention, both in design and in handling procedures. The Department of Defense and many informed companies place stringent design, handling, and packaging requirements on suppliers. However, to date, insufficient emphasis has been placed on properly managing a comprehensive program to mitigate the effects of ESD, and yet, the success of an ESD program depends heavily on how well it is managed.

A number of years ago, the ESD Association was asked to develop a static control standard to replace the existing U.S. Military, MIL STD 1686C. Pursuant to this request, and recognizing the need for compatibility with existing industry static control programs, the ESD Association released ANSI ESDA S20.20-1999 "Development of an Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies, and Equipment". This new standard defines the basic elements of a static control program, including those described below, and is compatible with the requirements of ISO 9000/14000 quality programs. The ESD Association has also trained ISO auditors to provide third party certification of the S20.20 program. [4] ESDA S20.20 is an excellent foundation for an ESD program and the benefits of this document are more fully realized when it is an integral part of a total system of program management.

Successful ESD program management requires a total system approach, one that is interwoven into every aspect of the manufacturing process from product design to customer acceptance. The interaction of electrostatics and manufacturing program

management are becoming recognized, however, there are a relatively small number of engineers and technicians possessing expertise in both areas.

PAST AND CURRENT APPROACHES

A wide variety of managerial approaches have been implemented over the years and have experienced a similar variation in success. Frequently, programs are implemented initially with considerable success only to fail years later. Once the control measures are in place and highly visible, a sense of accomplishment often leads management to move on to other manufacturing issues. The administrative and technical elements of the program then begin to erode and ultimately become ineffective. This deterioration may go unnoticed for some time due to the false sense of security created by the visible program elements such as wrist straps and tablemats. The ensuing return of high ESD failure rates often trigger a resurgence in managerial emphasis only to repeat the cycle of success followed by failure. Other programs never experience the success for a variety of reasons. These reasons are often the result of disproportionate emphasis on details such as the selection of ESD control products and not on the administrative aspects.

It is essential to recognize that ESD program management (EPM) has many elements and they must be coordinated and managed over long periods of time with a total system approach. There are as many ways to accomplish this as there are managerial techniques.

There is no doubt that the careful selection of a few static control methods can have an immediate positive effect on manufacturing results. However, if one is looking to maximize and sustain the positive results in the complex, rapidly changing manufacturing environment, more is required. Administrative elements and a total system approach must be added to the static control program. One approach [3] is outlined in Figure 1 and was the first program to become certified to ESDA S20.20 in the United States. A few elements common to most programs are described below in this paper.

TWELVE CRITICAL FACTORS OF ESD PROGRAM
MANAGEMENT EXCELLENCE

- **An effective implementation plan**
- **Management Commitment**
- **A long-term process owner**
- **An active leadership team**
- **Realistic requirements**
- **Training for measurable goals**
- **Auditing using scientific measures**
- **ESD test facilities**
- **A communications program**
- **Systemic planning**
- **Human factors engineering**
- **Continuous improvement**

Figure 1. A Systemic approach to EPM
(From ESD Program Management by T. Dangelmayer [3])

In creating these administrative elements, attention should be paid to the requirements of ESDA S20.20 and existing quality control standards, such as ISO 9000/14000. The static control program must conform to existing quality plan requirements and infrastructure to be successful.

Define the scope of the program – why there is a need for static control, what areas will be included, and what are the intended results. Testing or other types of analysis should establish the static charge sensitivity of the products being manufactured, as this is important to defining the extent and complexity of the static control program. Anyone looking at the program documentation should immediately understand why the program exists.

Program tasks, activities, and procedures will then need to be clearly defined. Definition of the technical elements and selection of the materials for static control falls into this category. For example, a decision needs to be made whether to accept vendor material specifications, or to do in-house laboratory or in situ testing. Appropriate instrumentation and test procedures need to be part of the plan. Installation methods and employee operating procedures are included. How often will employees check the effectiveness of their wrist strap grounders, monthly, daily, or continuously?

Audit procedures fall into this area as well. A static control program without adequate auditing is doomed to fail, usually placing considerable amounts of product at risk before the failure of the static control is noted. Auditing is also considered the binding force behind sound ESD program management, including the development of a list of items requiring verification. For each item, define the required measurement and its limits, as well as the measuring instrument and its calibration interval. Also important is to define the frequency of audit for each item, as this may vary greatly. The frequency of the audit for each technical item should be based on the item's tested durability and the risk to ESD sensitive products if the item fails to function. Audit frequency strongly depends on the seriousness of the static problem and the impact that each static control method has on that problem.

Preventive and Corrective action procedures will also need to be a part of the administrative plan to deal with deficiencies uncovered in the auditing process. These procedures are usually an integral part of any existing ISO 9000/14000 quality plan. Some problems are simply corrected by procedural changes, but in the worst case may require the isolation of product or product recalls. Management may be very concerned about the possibility of selling product to customers that has been damaged by ESD in the period between audits.

Employee training is another critical factor essential to the success of any process in a manufacturing area. All manufacturing personnel need to understand the goals, procedures, and technical elements of the static control program. Training will need to be done at the start of the program, and in response to audit findings. Regular refresher courses will also need to be scheduled, typically within two years of the initial training. The administrative section of the static control plan should define who needs to be trained, when the training should occur, and the type of training to be offered. Evaluation testing or certification needs to be included to demonstrate that the employee has the

required knowledge of the static control program. Training records for all employees will need to be maintained for accountability and to assure that knowledge of the static control program is current.

Support documents, usually industry standards, are the final administrative element. When specifying or developing these documents it is essential that they be realistic requirements for the production area. These documents support all aspects of the static control program, but particularly the technical elements and their audit procedures. Test methods, instrument calibration, and specification limits are typically contained in these documents. In the general field of static charge control, the ESD Association (www.esda.org) has an extensive range of documents addressing the testing of static control methods. Specialized documents on static charge control in the semiconductor industry are available from Semiconductor Equipment and Materials International (SEMI www.semi.org) and JEDEC (www.jedec.org). Static control standards for the disk drive industry are available from IDEMA (www.idema.org). Static control programs used in cleanrooms will likely have support documents that relate to contamination control aspects as well. All of the static control methods will need to be verified for their cleanroom compatibility. Support documents on particle shedding, chemical residues, and outgassing may be included.

LIMITATIONS AND TRENDS

Technology trends towards finer line widths and higher speeds are producing devices of ever-increasing ESD sensitivities (Class 0) and Charged Device Model (CDM) mitigation is becoming more challenging. For instance, automation is becoming commonplace and is often the cause of CDM failures. MR heads are known to have withstand voltages below 10 volts. At the same time, the introduction of ESDA S20.20 is raising the bar of expectations regarding handling practices. The Department of Defense and many informed companies are placing stringent design, handling, and packaging requirements on suppliers.

Furthermore, there are a relatively small number of engineers and technicians possessing expertise in both electrostatics and the administrative aspects of program management. The turnover rate of ESD Process Owners is high due to reasons such as career advancement and management not fully realizing the effort necessary to sustain success. This limitation is further complicated by the fact that knowledge of electrostatics and ESD is not commonly taught at universities and there are few sources of impartial technical training [1,2]. Rapid changes in the technology of products manufactured worldwide makes the development of appropriate static control knowledge even more challenging. Finally, management commitment to an ongoing static control program is difficult to secure when typical manufacturing operations have many other serious problems that need to be solved.

For many years, most companies have actively managed mitigation techniques for Human Body Model (HBM) damage. As a result, frequency of HBM failures has been greatly reduced. On the other hand, CDM mitigation techniques are less well understood and the opportunity for CDM events is far greater. The increasing use of automation is one significant source and the work place has many hazards such as static generating materials and surfaces that are too conductive. Understandably, CDM failure levels are the dominant failure mode today and well known industry authorities from integrated circuit suppliers such as IBM, Intel, AMD, TI, and ST Micro have indicated that they have been able to replicate the vast majority of their field return ESD failures with CDM

simulation techniques. CDM simulation test methods have improved considerably in recent years and commercial simulators are now available. More extensive training, however, is needed for better CDM mitigation results.

Automation greatly reduces human interaction with sensitive components and, therefore, reduces the likelihood of HBM damage. The contact, movement and separation associated with automation creates CDM risks and often the suppliers of automation equipment are not fully knowledgeable in CDM mitigation techniques either. The analysis of automation equipment for potential sources of ESD damage is significantly more technical as well. This is, therefore, another area where increased training is necessary.

The trends towards highly sensitive (Class 0) components such as MR heads are creating significant manufacturing challenges. With sensitivities below 10 volts, standard mitigation techniques are inadequate. Even the electrostatic measurement techniques are more complicated and technically challenging. Mitigation techniques involve considerable emphasis on avoiding metal-to-metal contact.

In response to these limitations, outsourcing portions of program management is becoming more common. In order to accommodate this, a number of ESD product suppliers are offering services related to ESDA S20.20 and the Association is delivering S20.20 training for consultants.

CONCLUSION:

Sound ESD program management is rapidly becoming a necessity and continues to be a significant challenge with growing demands. Many companies lack the expertise required to deal with the technology trends, automation, CDM mitigation techniques and the administrative elements. The limited resources for objective training are further complicating matters. Consequently, companies are either turning to outsourcing to gain the expertise or to developing internal resources with far greater commitments to program development and management. In either event, substantial training is required and generally difficult to acquire. Both consultants and ESD process owners internal to manufacturing companies would benefit from more aggressive and well-established training at Universities or within the industry.

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Chapter 3

Static Control Materials

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Abstract

Materials used within a program designed to control static electricity have not changed very much in fundamental properties in the past 10 years. Standards have evolved over the past decade to assist in the development of a conscientious static control program. Properties for non-ESD related physical characteristics have changed substantially in the same time period based on industry demands. This discussion will provide some insight into the requirements for materials used in a static control program as well as some general information about new materials that may have properties that may prove useful.

Standards and Specifications

Today, the users of static control materials have the benefit of industry standards to guide them in selection. Static control material suppliers also benefit from these standards, as there are fewer arguments about test methods, performance attributes and material specifications.

In 1990 there were no ESD related handling practices documents that enjoyed widespread acceptance. In the ensuing 10 years, various groups have prepared handling practices that are currently gaining in acceptance. There are three documents that the readers should become familiar with, as they will have an impact on the industry for many years. These documents are:

1. JESD 625A (update of EIA 625 - see www.jedec.org)
2. IEC TR 61340-5-1 (will replace EN 100015)
3. ANSI/ESD S 20.20 (commercial version of Mil STD 1686 - see www.esda.org)

Each of these handling practices documents contain tables that list almost every conceivable static control product or material and a suggested range of performance suited for the intended application. The specifications for static control products and materials involve an electrical property or a physical characteristic that imparts a static control property. The static control material types are listed below:

1. Static Dissipative
2. Static Conductive
3. Static Shielding
4. Static Discharge Shielding
5. Low-Charging (formerly known as Antistatic)

The definitions (by electrical or physical characteristic) for the above materials depend on the application. As an example, a static dissipative floor material has a different resistance range than a static dissipative packaging material. Also, the test methods vary between applications. Specifiers of static control materials must be aware of the different properties and test methods to ensure obtaining products and materials that meet not only the intended application but also meet the handling practice specifications they are referencing in their own ESD Control Program Plan.

Notice the new term, “Low-Charging”, that is listed as a replacement for the word “Antistatic”. This change has taken place in many of the handling practices documents because the term Antistatic has been misused and misapplied. The original discussion about eliminating the term Antistatic occurred in the IEC. All the member countries in IEC Technical Committee 101- Electrostatics agreed upon the phrase “Low-Charging”. The new phrase more accurately reflects the physical property that is sought after when designing interacting surfaces. In other words, this interaction should result in low static charge generation between surfaces that contact and separate. Of course that is the exact definition of Antistatic in older US standards such as EIA 541, the premier packaging material standard. Unfortunately, Antistatic is often used in a generic sense to describe the full-range of static control materials and products, which results in a great deal of confusion between specifiers and suppliers. Table 1 lists the currently accepted static control material types, definitions and test methods.

Material Type	Definition or Specification	Test Method(s)
Static Dissipative –Packaging	$\geq 1 \times 10^4 \Omega$ to $<1 \times 10^{11} \Omega$	ANSI/ESD S 11.11
Static Dissipative –Flooring, Worksurfaces and most other items	$\geq 1 \times 10^6 \Omega$ to $<1 \times 10^9 \Omega$ (Some specific items may have resistance levels up to $1 \times 10^{12} \Omega$)	ANSI/ESD S 7.1-Flooring ESD S 4.1 –Worksurfaces ESD S 2.1 – Garments Other Items– See ESDA Standards
Static Conductive –Packaging	$<1 \times 10^4 \Omega$ $<1 \times 10^4 \Omega$-cm	ESD S 11.12 ASTM D 991
Static Conductive-Flooring, Worksurfaces and other items	$< 1 \times 10^6 \Omega$ Lower Limits determined by local safety ordinances	As above in Static Dissipative
Wrist Strap Assemblies	$<3.5 \times 10^7 \Omega$ (Resistance to ground while worn) $<1 \times 10^7 \Omega$ (Resistance to ground while worn in very sensitive environments)	ESD S 1.1 – Wrist Straps
Static Shielding	<30 volts (Mil PRF 81705 for Type III materials)	EIA 541 Appendix E V-ZAP
Static Discharge Shielding	< 50 nJ <25nJ (in some company specifications)	ANSI/ESD S 11.31
Low Charging	Charge generation below the level that is estimated to cause damage in the application	ESD ADV 11.2 (Guidance)

Table 1 – Static Control Materials, Definitions and Test Methods

Test Methods

In the past 10 years, serious work has taken place in the standards development groups, especially the ESD Association, to create or refine test methods for static control materials and products. In 1990, a controversy existed over using ASTM D 257 for measurement of the surface resistivity of static dissipative materials. Today, ANSI/ESD S 11.11 is widely used for this purpose, although the results are expressed simply as ohms rather than ohms/square. International standards such as IEC 61340-4-1 also reference the methodology of S 11.11. These newer standards eliminate variables that caused confusion in using the ASTM method for the dissipative range of materials. Historically, more papers have been presented on problems of using ASTM D 257 for the dissipative range of materials than almost any other static control subject. Please note however, that ASTM D 257 is still recommended and used for its intended range – insulating materials.

ANSI/ESD S 11.31 measures static discharge shielding of bags based on energy seen inside the bag during the discharge event. This test method or a similar updated variant will be used in the upcoming revision of EIA 541 to replace the static-shielding test cited in Appendix E (V-ZAP- capacitive probe differential voltage test from 1988). The newer ESD Association method eliminates some significant variables associated with making a differential voltage measurement as described in the EIA document. Packaging material suppliers may continue to use both test methods since the information obtained by each of the methods is useful for quality assurance and material design purposes. Both test methods use a capacitive probe inserted into the package under test (bag or pouch). The EIA version uses two voltage probes that monitor the voltage on the top and bottom plates of the capacitive sensor. The observed voltage values are added together and the sum is reported as the peak voltage observed inside the package. The newer test from the ESD Association places a 500 Ω resistor across the plates of the capacitive sensor. A current probe measures the induced current flowing through the resistor. Generally, a computer program is used to calculate the resulting energy by integrating the area under the observed current waveform.

Charge generation testing has always been controversial and nothing is different today. There are no recognized (industry-wide accepted) methods for determining whether or not something has a low-charge generating propensity. The best that can be offered is to create a test that simulates the end use of the proposed static control material, in conjunction with the items or materials that it will contact. Many papers have been presented on this subject in the EOS/ESD Symposiums over the years. Interested readers are encouraged to look at Proceedings of the EOS/ESD Symposiums from 1990 to the present for more information. No values are shown in Table 1 for the charge generation level associated with the term "low-charging". This is because each application must have a definition of its own.

The end-user community is beginning to recognize resistance-to-ground as the appropriate measurement for most items used in the typical static control work environment. Installed floors, worksurfaces, chairs, shelving units, carts, people and any other conductive or dissipative item may be evaluated for static control performance by measuring resistance to ground. Resistance between two points is a measurement

used to compare materials during the selection process and to evaluate items like garments, chairs, wrist strap components, shoes etc. Some element of care is needed to select the appropriate test method. Of course, to avoid disagreement, it is best to use tests that have industry recognition.

An old test method called static decay is still widely referenced but is controversial. Static decay can be used to give an indication of the charge draining characteristic of materials but some experts in the field will argue that resistance measurements can provide the same information. In some cases though, resistance measurements alone may not predict how an item may react when electrically charged and then brought into contact with ground. Static decay testing may provide information about the dynamic nature of charge mobility on an item that resistance tests (with defined voltage and current) cannot provide. The main argument in the industry relates to how the item under evaluation receives the charge. The methods generally discussed include DC (power supply contact charging), triboelectric charging (contact and separation with some other material) and corona discharge (non-contact charging). The measurement of the charge decay of an item or sample of a material is relatively straightforward using a non-contacting voltmeter, electric-field meter or other such device, along with some sort of timer. Please note however that charge decay testing is really only meaningful on homogeneous materials. Testing composite materials or laminated structures results in information that may be difficult to interpret since the most conductive path or layer in the material will control the result.

Material and Product Performance Requirements Today

Perhaps the electronics industry can be segmented today as follows:

1. General Electronic Assembly
2. Semiconductor Manufacturing
3. Disk Drive Manufacturing
4. Flat Panel Display

While many would (perhaps rightfully) argue that the above list is an oversimplification of the complex world of electronics, this should be viewed as only an example to allow a reasonable discussion about static control material properties that are important within the broad industry segments. In addition, other physical properties often affect the acceptability of a given item or material within these broad industry segments.

Interestingly enough, the static control properties and performance specifications have not changed a great deal over the past 10 years but the actual products and materials have changed dramatically. This is due to the other physical and chemical property requirements demanded by end-users. All the industry segments have requirements for cleanliness, ionic content, outgassing and water vapor transmission that were rarely discussed just 10 years ago. These "other" requirements are driving the material and product changes far more than the static control property considerations. The difficulty from the static control material design point of view is "how to obtain or keep the static control property and be clean at the same time". It is important to understand that one of the reasons the demand for cleanliness is so great today is because of the ease (relatively speaking) to detect infinitesimally small amounts of anything on a surface. Can 20 nanograms per square centimeter of sodium or nitrate ion on a packaging material really cause a problem? The almost magical detection ability is great for

forensic science but is it really necessary to demand that a wrist strap band material not contain common ionic levels above a few micrograms? If that's the case then how can people that have to wear a wristband be allowed in the work area? People are obviously far more contaminating than a wristband. It would be helpful to the industry overall to see some scientifically sound proof, presented in an appropriate peer-reviewed forum that shows that the cleanliness requirements demanded today by many manufacturers are truly needed.

A "material design triangle" for the industry appears in Figure 1. Pick any two attributes and the third will not be (readily) available. While this is obviously a bit cynical, it is shown to make a point about material properties; that being, it is difficult to do everything for everyone without some give and take regarding specifications.

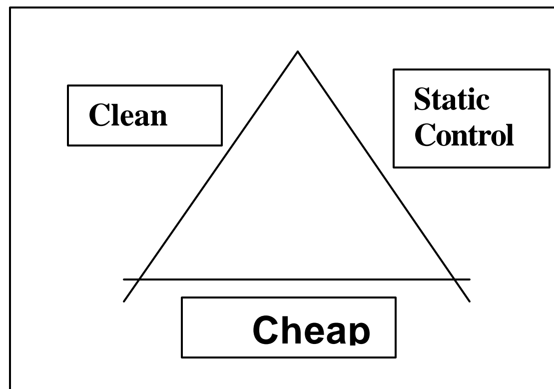

Figure 1 – Material Design Triangle

Pick 2	Result
1. Static Control and Cheap	– it probably won't be Clean
2. Clean and Cheap	– it won't have much Static Control
3. Static Control and Clean	– it most assuredly won't be Cheap

Recent Advances in Materials for Static Control

This article will not be able to do justice to the most recent advances in static control materials so the reader is encouraged to review the advertisements of material suppliers. In addition, watch for papers presented in industry forums such as the EOS/ESD Symposium (see www.esda.org for this year's Symposium details).

Of major importance today is the commercialization of materials that meet the definition of intrinsically conducting polymers or ICPs. These polymer-based materials are similar to semiconductors in that a stable matrix has been modified with a "dopant" additive that allows conduction through the (insulating) polymeric matrix. This of course is very different than bulk loading of conductive powder, fiber or crystalline materials into a polymer during the melt phase to create a bulk conducting material. Continued development of ICPs will result in new materials that are cost competitive, stable and far more useful than the earlier (1980s and early 1990s) available materials. Keep a close watch on the industry to see if a material appears that may be useful to your applications. The ability to maintain a clean surface is a benefit of this class of material.

Coatings and surface treatments to modify the electrical or triboelectric (charge generating) properties of material surfaces have been used for well over 30 years. The need to provide surface electrical resistance, lubricity and other modifications to reduce charge generation will continue. Factoring in the new requirements appearing in some segments of the electronics industry to provide low ionic content, low outgassing and reduced Non-Volatile-Residue (NVR), will remain a challenge to the material suppliers. It is not well understood in the electronics industry that reduction of static charge generation between any two contacting surfaces requires a certain amount of sharing of ionic species (chemicals) between the surfaces. These concerns apply to all sorts of static control products and materials including: worksurfaces, flooring, garments, grounding devices, packaging and containers, chairs, ionizer systems and anything else that enters the work environment.

While metallized surfaces for the purpose of static shielding or static discharge shielding are widely recognized and used systems, adding in the requirement of low water vapor transmission (WVTR) has impacted the idea of transparency in packaging materials. Most conventional and reasonably priced moisture barrier films have a heavy aluminum layer that results in an opaque package. While it is possible to provide low WVTR in a clear film using special materials, the cost is prohibitive for all but the most sophisticated applications. If static discharge shielding is also required in the clear film then the cost goes up substantially.

Low outgassing is a consideration for all materials that enter a cleanroom. Reducing the volatile components from all the items that enter a cleanroom is a logical cleanliness requirement but one that has cost and static control performance implications. Many of the additives that provide low charge generation characteristics or the static dissipative property have considerable outgassing levels that cannot be avoided. Naturally, some newer technologies may be able to show reduced or in some cases acceptable levels of outgassing for many applications. However, as stated previously, it is time to have some proof that all the cleanliness related specifications imposed by users of static control materials are really necessary.

Conclusion

Handling electronic parts requires an electrostatic protected area or EPA. This concept is universal among the recent handling practices documents prepared by the Electronic Industry Alliance (EIA/JEDEC), the International Electrotechnical Commission (IEC) and the Electrostatic Discharge Association (ESDA). Static control material properties as defined in the handling practice documents and their specifications are fairly well harmonized. Only small variations exist that should be relatively easy to work around in any well thought out static control plan.

Cleanliness issues require careful, thoughtful and reasonable consideration during the process of establishing material specifications. It must be understood that in most cases the static control attributes for many products will be provided at the expense of cleanliness. Some new materials claim low contamination levels while maintaining static control properties in the static dissipative or static conductive range. The reader should investigate material properties based on the realistic and necessary application requirements.

Chapter 4

ESD Control With Ionization

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INTRODUCTION

Electrostatic charge attracts contamination to surfaces of semiconductor wafers and flat panel displays, as well as to critical surfaces of process tools. Electrostatic discharge (ESD) damages electronic components as well as the tools used to manufacture them (for example, semiconductor photomasks). Electrostatic charge also causes malfunctions and handling problems in the automated production equipment.[1]

The ESD sensitivity of semiconductor components is routinely decreasing with each succeeding semiconductor generation. While typical damage thresholds for semiconductors may range from 50 volts to over 10,000 volts, ESD sensitivities for GMR heads in the disk drive are already under 5 volts. Technology trends in all areas of electronics production will make existing static problems worse.

STATIC CHARGE CONTROL WITH IONIZATION

Static charge generation is unavoidable. Triboelectric charging occurs through the contact and separation of materials. A charged surface can also induce an electrostatic potential (voltage) on conductive objects close to the static charge without any actual contact. Avoiding charge generation and transfer throughout the electronics manufacturing process is essentially impossible, but with a comprehensive program, it can be controlled. Every static control program starts with extensive grounding of all conductive and static dissipative materials including personnel.

Non-conductors are required in process areas (most often, they are the product itself). Since charged non-conductors will not consistently lose their charge by grounding, methods of neutralization are needed. Ionization is the most used technology for the neutralization of static charge on non-conductors and conductors that are isolated from ground. Room ionizers provide neutralization over large areas, worksurface ionizers target smaller production areas, and point-of-use ionizers are included in production equipment. Ionizers used in electronics production areas must follow the same general guidelines for material compatibility as other equipment in the area. Cleanrooms have their special requirements and there are several types of ionizers qualified for the most exacting requirements of Class 1 and better cleanrooms.

ISSUES FOR STATIC CHARGE CONTROL

Technology development in many areas is making the control of ionizers more critical as their use is becoming more essential. Trends in semiconductors to shrinking geometries, more dense devices, and an increasing number of I/O pins assures that ESD damage thresholds will decrease. Sooner or later ICs will reach a technology barrier, as was found in disk drive assembly. It is not now possible to produce disk drives without ionization to protect the GMR heads from ESD. Device density is pushing power consumption, leading to decreased power supply voltages and noise margins. Electronic devices will become more sensitive to electromagnetic interference (EMI) as the result, and equipment interruptions more frequent. Shrinking geometry also means shrinking killer particle sizes and smaller particles are easier to attract with static charge.

Ionizer Balance — Ionizer balance (offset voltage) needs to be maintained at low levels to avoid charging sensitive isolated conductors. Unfortunately, there is no simple way to relate ESD sensitivity to ionizer balance measurements made with the Charged Plate Monitor (CPM) of ESDA standard, ESD STM3.1. [2] Designed for semiconductor applications, the CPM may not be appropriate to indicate ionizer balance at low levels or on small objects. The CPM measures balance on a 150mm square, isolated, 20-picofarad conductive plate, which might look like a semiconductor wafer, but hardly reflects the dimensions or capacitance of disk drive components or flat panel displays. Further, ionizer balance measured by the CPM does not reflect the voltage that the ionizer may induce on other objects. In addition, the CPM design fixes the plate within 25mm of ground. Real objects are rarely under this constraint and will have different ionizer induced voltages.[3]

Ionizer balance below 100 volts is occasionally required for semiconductor applications, while balance to 5 volts and less is required for GMR technologies. Most CPMs have questionable accuracy and measurement stability in this low range. While able to measure the balance of a DC ionizer, CPMs do not have the frequency response to measure the voltage swing of an AC ionizer. At best, they indicate an average value of the AC ionizer balance, leaving the ESD-sensitive component exposed to higher AC voltage swings that are actually occurring. Isolating the ESD-sensitive devices from the AC ionizer by distance has worked, but decreasing device damage thresholds may make this impossible in the future.

Cleanroom Compatibility and Air Turbulence — Fast neutralization of static charge to prevent ESD requires either high airflow or a short distance between the ionizer and the ESD-sensitive component. Current cleanroom designs are reducing airflow to reduce energy costs. In some applications cleanroom airflow rates are already inadequate for fast neutralization and ionizing blowers augment the airflow. Careful selection of these blowers is required to minimize contamination problems. Attention must be paid to the ionizer's internal design, fan type and other material issues to avoid generating particle and chemical contamination. Meeting the increasingly stringent requirements of the cleanroom will inevitably increase the cost of ionizers and other static control methods.

Ionizer Maintenance — All ionizers will require some type of periodic maintenance. This usually involves cleaning the ionizer emitter points and checking or adjusting the ionizer balance every 3-6 months. Extremely critical applications involving GMR heads may require checking the ionizer balance more frequently, possibly at 1-month intervals or less. Ionizer maintenance depends on the presence of airborne molecular contaminants (AMCs) that cause particle growth on the ionizer emitter points resulting in ionizer balance changes. As AMCs affect other aspects of cleanroom electronics production, they are increasingly controlled by efficient air filtration systems. At the very least, the result will be reduced ionizer maintenance requirements.

CHALLENGES

Most current ionization techniques used in electronics production are electronic, employing corona ionization. Efficient designs, providing sufficient ion densities for fast neutralization, use the AC, steady-state DC, and pulsed DC technologies currently available. Increasing future requirements for low levels of ionizer balance require the use of sophisticated methods of monitoring and feedback control. We have already learned in disk drive production that there is a practical limit of about 3-5 volts in control of corona ionizer balance. This has produced a shift to the use of alpha or soft x-ray ionizers. Physics dictates that these ionizers produce a continuous balance of positive and negative ions without feedback and control methods. They will find increasing uses in applications requiring low levels of ionizer balance, particularly in industries shifting to automated production techniques. Maintenance of these ionizers involves the periodic replacement of their active elements and compliance with the applicable government regulations.

Measuring methods of ionization may need to be changed to better represent the range of sizes of ESD sensitive components. Static charge issues for a one-meter square of glass (flat panel display) are very different than for a GMR head, and neither is adequately represented by measurements made with a CPM. Yield analysis needs to establish requirements for ionizer balance, as well as the applicability of existing ionizer technologies (particularly AC ionizers) in handling extremely static-sensitive components.

Close attention must also be paid to turbulence generation by the ionizer. Cleanrooms use laminar airflow to prevent particle deposition on critical surfaces. The use of ionizing blowers or other ionizers placed in the airflow path means that turbulence could compromise the laminarity of the airflow. Therefore, bar ionizers, ionizing blowers or other types of ionizers must be carefully selected to minimize this effect. The cleanroom compromises between contamination control and ESD control must be well understood.

The following are some recommendations that will assist manufacturers of ionizer products in updating equipment specifications:

1. Establish the "real" damage thresholds of electronic devices with a well-defined testing program, including simulation methods that reflect the ESD hazards that devices will encounter. For example, the increasing use of automation tends toward CDM and MM testing rather than HBM. Estimate how sensitive devices will be in the future.

2. Establish ionizer neutralization time and balance specifications for standard airflow rates (both laminar and turbulent) and operating distances. Relate this information, if possible, to production yield or defect rates.

3. Define requirements for cleanroom compatibility, reliability and maintenance for all ionizers. [4]

CONCLUSION

Ionization continues to be an essential element in a static control program. As with other elements in the program, control of the operating parameters will become more critical with technological change. Product design to maximize ESD damage thresholds may not be able to keep up with this rapid change, putting more dependence on ionizers and other static control methods to protect products. In all areas we are looking at rapidly approaching technology barriers. Surmounting these barriers means, "static control is not an option". Ionizers and ESD control methods will need to keep pace with rapid technology change or they will become the barriers to future production.

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Chapter 5

ESD Control in Cleanrooms

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Introduction

Static charge control has become a necessity in cleanroom environments. Static charge is a contaminant that must be eliminated to enhance the production of semiconductors, disk drives, flat panel displays, medical and optical devices, commercial/military/ aerospace technology, and a variety of other products. By controlling static charge, it is possible to:

1. Protect against product contamination due to electrostatic attraction (ESA) and bonding of particulate to critical product surfaces.
2. Prevent product handling problems of materials and media caused by ESA and allow higher process speeds.
3. Prevent damage done directly to products by electrostatic discharge (ESD).
4. Prevent the malfunction of production equipment caused by ESD.

Besides their ability to dissipate electrostatic charge and prevent charge generation (triboelectrification), static control methods in cleanroom and clean manufacturing environments must consider the issues of particle generation, chemical compatibility, and outgassing.

Electrostatic Attraction (ESA)

Cleanrooms exist because particles on critical product surfaces cause defects. Particles will create defects and damage to a thin film when it is deposited on a substrate, whether permanently as part of the product, or temporarily as part of the process. The problem is the same for oxide coatings on semiconductor wafers as it is for paint on car bodies. Particle related defects may require the product to be reprocessed, or they may cause a catastrophic failure. In either case, this creates a reject that lowers the overall yield of the production process.

Lowering airborne particle counts with high quality air filtration and laminar airflow is the method used in cleanrooms to reduce surface contamination. Modern filtration efficiency can be quite good, and few damaging particles penetrate the air filtration system. Most particle problems are caused by particles generated within the cleanroom by personnel, equipment, and production processes. Unfortunately, these particle sources are located close to the product.

Numerous researchers have demonstrated the connection between static charge on surfaces, and attraction and bonding of particulates. Neutralizing static charges on

critical surfaces will reduce the propensity for electrostatic attraction (ESA) and bonding of particles to these surfaces. Eliminating static charge can enhance the ability of the air filtration system to remove particles from the cleanroom environment, since particles will remain in the laminar airflow, rather than depositing on surfaces.

ESA makes some cleanroom products difficult to handle, for example, small mass semiconductor parts or plastic films. If small parts are involved, they may migrate from, or stick to, where they are placed. This may interfere with subsequent operations, particularly when robotic handling is involved. Plastic webs may take on high static charges and break or jam. Highly charged materials are difficult to join or laminate. Fine powders and media do not convey well.

Electrostatic Discharge (ESD)

Many static charge-related problems are the result of electrostatic discharge (ESD). The most common results of an ESD event are damage done directly to static sensitive products, and production line downtime caused by malfunctions of equipment. Examples of this are common in, but not limited to the semiconductor electronics industry, electronic products manufacturing, and conveyance equipment.

In semiconductor electronics production, smaller device geometries have evolved from the need for increased performance and higher operating speeds. This has resulted in a higher density of individual devices on a semiconductor wafer. ESD events cause failures of devices through the vaporization of metal lines, the punch through of thin oxide layers, or other failure modes. Even worse, ESD events can weaken devices so that they still pass production testing, but fail prematurely when installed in a user's equipment. Products in the medical, optical, and film industries are also known to be sensitive to the occurrence of ESD events. Whenever thin films are deposited on substrates, they may be damaged by ESD. ESD creates severe problems with the photomasks used to produce the patterns on the semiconductor wafer. These photomasks consist of isolated chrome film conductors on a quartz substrate. Photomasks damaged by ESD produce repeating defects on the wafer surface, leading to large numbers of defective devices.

Besides damaging product, ESD events can affect the equipment that makes the product. Many types of production equipment use microprocessors for control. ESD events can interfere with the operation of this equipment, and are often mistaken for “software glitches”. ESD events also create a significant amount of electromagnetic interference, or EMI. It is possible that an ESD event in one piece of equipment could affect the operation of adjacent equipment. As cleanrooms become increasingly automated, their operations are often controlled by a computerized factory management system (FMS). An ESD event can create bad data in one piece of equipment that can affect operations throughout the cleanroom. While usually not catastrophic, machine shutdowns cause production line downtime, reduced process speeds, and occasional product losses. Inefficiencies in the production process always result in higher production costs.

Charge Generation in the Cleanroom

The nature of operations in the cleanroom encourages the generation of static charge. Typically, charge is generated whenever two dissimilar materials are placed in contact and then separated. The amount of charge generation is affected by several factors including the types of materials, their surface conditions, ambient humidity, pressure of contact, and speed of separation. Also important is the availability of path to ground for any charge generated on conductive materials.

Cleanrooms make extensive use of insulating materials. Cleanliness and chemical process requirements in the cleanroom require the use of glass, Teflon, Kynar and other plastics. Personnel are enclosed in cleanroom garments, booties, and gloves, also made of insulating materials. Hard smooth insulator surfaces, required for easy cleaning, generate high charges. The clean surfaces of most cleanroom materials do not provide leakage paths for charge to flow to ground. Most cleanrooms control humidity levels at 45%RH or less. These low levels of humidity encourage triboelectric charge generation and provide very slow rates of dissipation once the charge has been generated. Throughout the manufacturing process in the cleanroom, materials, personnel, and equipment parts are in motion, in contact with each other, and constantly generating static charge.

Solving Cleanroom Static Charge Problems

Many devices exist for preventing or dissipating static charge on materials, personnel, equipment, and facility surfaces. Wrist straps, conductive shoes and floors, and dissipative or conductive construction and furniture materials are common methods in work areas outside cleanrooms. They all work by providing a path to ground for the charge generated on the object. If the path to ground is continuous, it will not only remove static charge, but also limit the amount of charge that may be generated. For example, limiting the resistance to ground for materials to a range of less than 10^9 ohms and greater than 250k ohms will generally assure that the potential due to charge on the objects does not exceed 100 volts.

Cleanroom static control should begin when the facility is under design consideration and construction. Static control considerations apply to the walls, floors, windows, and ceiling components (including lighting fixtures) of the clean environment as well as means of ingress or egress, anterooms, gowning areas, air showers, etc. As much as possible without compromising structural, contamination control, or process requirements, clean environment construction materials should be conductive or static dissipative. They should be provided with a path to ground that is verified during the construction process, and periodically thereafter. Attention should be paid to the fastening methods that connect walls, floors, and ceiling components to assure that a reliable ground path is maintained. See ESD S6.1 Grounding, ESD STM4.1 Worksurfaces – Resistive Characterization, ESD STM4.2 Worksurfaces – Charge Dissipation Characteristics, and ESD ADV 11.2 Triboelectric Charge Generation for methods of testing the static control characteristics of construction materials.

An isolated conductor is often more of a hazard to products or equipment than an insulator since it has the ability to transfer all of its charge in a single ESD event. Avoid conductive materials that have an insulating coating or paint applied to them when possible. The coating may charge and then induce charge on the conductor. If the

coating is thin or damaged, the result can be ESD events to nearby conductive items (devices) or grounded surfaces.

Cleanroom construction materials will have to pass all the facility requirements for contamination control. Specifying a conductive or static dissipative resistance range for a material may limit the available choices. Protecting sensitive components from ESD may require the use of static dissipative materials in construction applications where conductive materials are preferred for other reasons.

The need for contamination control makes some static control methods difficult or impossible to use in cleanrooms. For example, cleanroom garments are used to completely enclose personnel to prevent personnel generated particles from entering the cleanroom work area. The materials used in these cleanroom outer garments, including shoes, booties, and gloves, are often insulating materials capable of generating high levels of static charge when they contact other garment materials worn by personnel. Charge is generated on both the inside and outside of the garments, as well as on personnel wearing the garments. Insulating gloves will generally charge materials and items that personnel handle during production. Providing a reliable path to ground for all garment elements can be a challenge.

Static dissipative materials are generally created by adding conductive materials or chemicals to insulative polymers and elastomers. These may be carbon or metallic powders, chemicals that leach to the surface to create a conductive path, or hygroscopic chemicals that attract water to the surface of a material. In all of these cases, the method of creating the static dissipative property may be a potential cleanroom contaminant. Continuous cleaning of cleanroom materials, particularly the washing of garments, may cause them to lose their static control properties over time. All cleanroom materials will need to be monitored periodically for effectiveness, and replaced as needed.

Eliminating or isolating insulators in cleanrooms may be impossible. Insulators are usually a part of the products being produced in the cleanroom. Oxide-coated silicon and epoxy packaging in semiconductors and glass flat panel display screens are good examples. Insulators may also be required for high temperature operations or chemical resistance. When insulators cannot be eliminated or isolated from static-sensitive products, the most common methods of static control are high humidity (condensation), chemical coatings, and air ionization. The first two methods rely on providing a discharge path to ground along the surface of the insulator.

Air ionizers use the air as a means of bringing opposite polarity charged gas molecules to neutralize charge on insulator surfaces. High humidity levels and chemical surface treatment treatments are often not compatible with cleanroom operations. In most cleanrooms, the only acceptable method for controlling static charge on insulators and isolated conductors will be air ionization. Air ionization may be incorporated as a part of the clean laminar airflow in the cleanroom or clean enclosure to neutralize static charge on stationary or slowly-moving surfaces. Point-of-use air ionization using fans or compressed gases may be required for faster moving equipment surfaces and product transport charge neutralization.

Contamination Control Considerations

Contamination control requirements will need to be part of the selection process for static control methods used in cleanrooms. Chemical or thermal characteristics necessary for some manufacturing processes also limit the choice of static control methods. Many static control methods make use of static dissipative or conductive materials that contain additives to the insulative base materials. As with any other object brought into a cleanroom, these materials must demonstrate cleanroom compatibility. This involves testing for particle shedding (particularly since some materials use carbon or metallic particles or fibers to achieve the desired conductivity) of both new materials and those that have undergone some period of cleanroom use. Ionizers used in cleanrooms will need to satisfy the same contamination control requirements as other materials used in the cleanroom.

"Sloughing" is the process of shedding particles by a material when it is flexed or abraded. This occurs on virtually all "plastic" packaging materials to a greater or lesser degree depending on the durometer hardness of the "plastic". The sloughed particles tend to be a cleanroom contaminant, although they are generally chemically inert. In this case, the particle size of the sloughed particles is the principal concern. The carbon or metallic additives used to create conductive and static dissipative materials are chemically active, so that particles of any size sloughed from these materials may be a contamination issue.

Particulate testing for sloughing involves washing the material with deionized water or another appropriate solvent, and uses liquid particle counters, or ion and gas chromatography to identify and measure particle element, quantity and size. Refer to ASTM F312 for a particle sloughing test methodology.

Contamination issues are not limited to particles, but include chemical compatibility, outgassing of volatile chemicals, and other unwanted residues from processing additives. These requirements include:

1. Ionic contamination – This testing looks for contamination that is not electrically neutral but is charged either positively or negatively. Typical ionic contaminants are the anions – fluorine, chlorine, bromides, nitrates, nitrites, phosphates, and sulfates as well as the cations – lithium, sodium, ammonium, potassium, magnesium, and calcium. The main problem with ionic contamination is that it causes corrosion. Ionic contaminants are determined by chromatography and reported in ppm (parts per million).

2. NVR Testing - The filtered solvent from particulate testing is used to determine the presence of any chemical surface residues. The sample is heated to evaporate the solvent and analyzed for total remaining non-volatile residue. The residue may also be analyzed to determine its chemical composition.

3. Outgassing - Head Space Analysis for volatile chemicals is performed using gas chromatography/mass spectrometer. The material sample is heated in a closed container, driving off volatile components. The collected sample is then analyzed by weight. Refer to ASTM E595 for a test methodology.

Air ionizers used in cleanrooms should demonstrate compatibility with the cleanrooms in which they are used. All ionizer components installed in the cleanroom should meet the same contamination control requirements as other materials in the cleanroom, and should be capable of passing the cleanroom tests described above. It is particularly important to choose ionizer emitter point materials that are appropriate for their use in a cleanroom manufacturing process. In addition, operation of ionizers in the cleanrooms requires attention to issues of EMI generation, ozone, and air turbulence from fans or compressed gas supplies. Cleanrooms have their special requirements and there are several types of ionizers qualified for the most exacting requirements of Class 1 and better cleanrooms.

Challenges for Static Charge Control in Cleanrooms

Technology development in many areas is making static control more critical. Trends in semiconductors to shrinking geometries, more dense devices, and an increasing number of I/O pins assures that ESD damage thresholds will decrease. For example, it is not possible to produce disk drives without a full static control program including ionization to protect the GMR heads from ESD at voltages of 5 volts or less. Device density is pushing power consumption and heat generation, leading to decreased power supply voltages and noise margins. As a result, electronic devices will become more sensitive to electromagnetic interference (EMI), and equipment interruptions due to ESD may become more frequent. Shrinking device geometry also means shrinking "killer" particle sizes. Smaller size particle contaminants can be easier to attract with lower charge levels and related lower electric field intensities.

Cleanroom facilities are becoming larger and more complex, assuring that difficulties in adequately grounding materials in the cleanroom will also increase. Process acceptable chemical and molecular contamination levels continue to become lower, narrowing the ranges of cleanroom compatible materials, particularly those with static dissipative properties. Cleanroom designs with high ceilings and less than 100% HEPA filter coverage makes the application of ionizers more difficult. Equipment manufacturers will face similar difficulties in producing static safe designs of their equipment. Meeting the increasingly stringent requirements of the cleanroom will inevitably increase the cost of all static control methods. As the use of static control methods expands in the cleanroom, so will the costs of auditing their performance and administering the overall static control program. Fortunately, the return on investment of the static control program is many times the program cost.

Conclusion

ESD control methods, grounding, material selection, and ionization, will need to keep pace with rapid technology changes or they will become the barriers to future production. Nowhere is this more apparent than in the cleanrooms where our high technology products are produced. Product technology change drives changes in cleanroom design, and the manufacturers of static control equipment must recognize these changes. Static control methods must be cleanroom compatible. There also needs to be a better understanding that good static control design and proper handling of devices during assembly cannot compensate for ESD damage during device manufacture in cleanrooms. Increasingly, "static control is not an option".

Chapter 6

Component Level ESD Challenges

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Introduction

Electrostatic discharge (ESD) component/device/IC level stress testing continues to be a critical step in the qualification process of electronic products like integrated circuits (ICs). In 1998, SEMATECH rated ESD as the #3 in the list of future problems related to yield and device reliability [3]. Technology development is making ESD testing more challenging because the testers must continue to improve to account for the demands of larger pin counts of the devices. Pin counts have gone from 168 to greater than 1000 pins in the last 10 years. The SEMATECH roadmap points to IC packages with as many as 5000 pins in a few years [3].

Even though the trend is toward total automation, the threat from the electrostatic discharge event will never go away. Designing against these increased threats will continue and this is what will continue to drive the ESD stress testing that is used to confirm that the goal of improving the ESD susceptibility has been achieved. This is even more important when we consider that ESD robustness is a key objective in the qualification and reliability of IC components and devices.

Device Models and ESD Test Standard Methods

The ESD Stress testing of components is needed because the results indirectly provide information about the level of susceptibility and/or immunity of all the pins on the product. The testing provides a benchmark against other products because the different devices are assumed to be tested under the same conditions as prescribed by the industry standard. The testing provides a useful comparison because “not all devices are created equal” and so, when the ESD testing is combined with ESD failure analysis, they can be used to determine the exact location and root cause of the ESD failures [4, 5, 6, 7, 8].

ESD Stress Testing has been done and is still being done using the three established and traditional ESD events called the Human Body Model [HBM], the Machine Model [MM] and the Charged Device Model [CDM]. These existing industry standards [9, 10, 11] provide guidelines for the methods so that the procedures are consistent no matter where the ESD stress testing is done and who does the stress testing. These established standards also provide for consistent results if all equipment/simulators being used meet the established industry standards requirement for operation.

These models differ however, in that HBM and MM simulate the electrostatic transfer of a charge (from a human or machine respectively) to the pin of the device, whereas CDM simulates the electrostatic transfer of a charge from the device [1]. The latter CDM test

method is intended to simulate discharge events that occur when a charged IC discharges directly through one of its pins into a low impedance ground. This is because real-world CDM events do occur during automatic handling or placements of ICs during manufacturing operations.

The current testing approaches allow a set number of devices from each technology and /or process to be tested at several voltages and or current levels. Susceptibility is determined at the failure level [9, 10, 11] for each model. The generally acceptable pass levels are for HBM 2000 V [9], for CDM 1000 V [11] and for MM 200 V [10]. Any number below these for the individual event is regarded as being susceptible for that event.

ESD Device Testing Challenges

The current limitation for ESD stress testing is also associated with increased device pin count. Pin counts have gone from 168 to over 1000 over the last 5-10 years. The Sematech roadmap [3] points to 5000 pins in a few years. As pin counts increase, the time for testing increases exponentially and this is because of the added possible pin combinations [12]. For any desired improved throughput, if testing is done with lower number of pin combinations, it leaves a hole in the testing process, and it is possible for weaker pins to escape testing and get into the field [13], thus creating a "walking wounded" or latent failure situation.

Technology development is making ESD testing challenging because the testers must improve to account for the demands of larger pin counts of the devices [1, 4]. Data collecting instruments (scopes and current probes) must also improve to measure the very fast responses {<<< than 10 nsec} of the device to the many ESD events [15, 16].

IC chip advances are making it difficult to test because as the complexity of the semiconductor chip increases, the required larger pin counts create additional internal interactions. The increased internal interaction between nodes at the silicon level is making it difficult to determine the exact usefulness and the extent of the usefulness to test all pin combinations. This increased internal reaction increases the risk of ESD damage in the core of the device for both HBM and CDM ESD events and most probably, the MM event [14] as well. These competing effects from the three distinct ESD events tend to increase the development cycles between designing, testing and bringing product to market in a timely manner.

Future Work

To overcome some of these problems, improved ESD testing methods must include Transmission Line Pulse {TLP} testing [17, 18] not only at the wafer level but also after the device has been packaged for qualification like burn-in. Although TLP testing has been around since 1985 [19] its level of use is still mostly confined to the select few using in-house-built TLP simulators. A standard method or standard practice document [20, 21] will be useful in the near future if not sooner because the method provides direct insight into the susceptibility of the actual ESD protection structures. This is mainly because the TLP data is quantitative, the discharge occurs in a relay (no air-arc discharge) and the method is easily extended to the wafer level testing [14]. In addition, the transmission lines are capable of producing very precise, high current, square or rectangular pulses with well-defined impedances.

If we now look at the relatively new effects, we see an almost direct correlation [22] between the TLP testing done at the engineering/wafer level or development stage and the HBM testing which is done for qualification (packaged product). Another reason why TLP is needed is that the DC breakdown voltage of ultra thin gate oxides falls below the breakdown trigger voltage of regular p-n junctions and this reduces the safety margin for protection schemes [17,18]. The traditional HBM ESD testing cannot provide this information because it is a Go/No-Go test; that is, it provides no insight to the physical behavior of the ESD protection structure.

ESD stress testing will be more challenging in the future because the ESD standards are not keeping pace with the increasing product types and packaging types [14, 23]. New ESD models could include the ESD testing of unpackaged wafers, in-package die, packaged silicon die, card level and board level. New ESD test methods like wafer level ESD testing (lot-to-lot and wafer to wafer comparisons) could help to accelerate the learning prior to final packaging of the die for qualification.

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Chapter 7

ESD Characterization

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For proper on-chip ESD protection design it is important to characterize the physical behavior of the silicon IC, as well as its circuits and sub-circuits. Such characterization can be used to assist computer simulations, or alternatively, to enable analytical ESD design.

Computer work includes compact modeling and simulation. It consists of carefully modeling the different sub-elements of a silicon design (such as e.g. individual NMOS transistors, diodes and metal busses) to subsequently simulate the physical behavior of a circuit composed of such sub-elements. Within the simulations, physical parameters that are not (easily) accessible in a silicon design and testing can be analyzed and studied. [1-2].

The analytical design methodology is the building of an ESD protection circuit with a convoluted response that is synthesized from the individual known (measured) silicon element responses. The key to success lies in the proper and complete characterization of the silicon technology and devices for typical ESD stress conditions.

Both simulation and analytical design are important approaches to avoid costly silicon re-designs. A full set of masks for one production run in 0.10um CMOS easily exceeds a cost of half-one-million US dollars.

Both methods require considerable skill and experience, as well as the production of silicon samples. Simulation work is very time consuming before the first result is obtained and it requires proper modeling and calibration. Models are not universally available and have limited validity in terms of maximum operation current and temperature, both significantly below the typical ESD conditions. Analytical design can be much faster, however it requires significant upfront work for proper test chip design, analysis and rule extraction.

Classification

The industry uses three major models to classify integrated circuits (ICs) for their ESD sensitivity: HBM (Human Body Model), MM (Machine Model) and CDM (Charged Device Model). This is a straightforward method to characterize the IC. However, this is too limited for the on-chip ESD protection designer since it only reveals a pass and fail

voltage while it does not provide for insight into the physical behavior of the (ESD) circuits under ESD stress conditions.

DC characterization

More insight into the physical behavior can be gained from simple DC measurements on the entire IC, but more preferably, on isolated circuits and sub-circuits.

DC measurements are easy to perform and do not require specialized equipment beyond equipment that is normally available in a standard IC measurement lab (curve tracer, parameter analyzer, or even simple current, voltage and resistance measurement equipment). With DC measurements, one can assess several ESD design parameters, such as the worst case breakdown voltage of a junction and a dielectric material, as well as bipolar model parameters such as multiplication factors and bipolar current gain. [3].

The limitations of DC characterization can be summarized as follows. First, DC measurements are limited due to Joule heating (power dissipation of a current flowing through resistance = I^2R) in the semiconductor device. From the classic Wunsch-Bell [4], the well-established curve that relates the power-to-failure to time-to-failure in silicon, it is known that failure power decreases as $1/t^{1/2}$ As such, one can deduce the expected DC power-to-failure: it is much lower than the power that can be dissipated during shorter stress times, such as ESD stress events. During relatively long DC measurements (seconds to minutes) the total dissipated energy (power x time) will be rather high for relatively low current levels. In other words, one cannot measure in the high ESD current range, without first destroying the silicon device-under-DC-test.

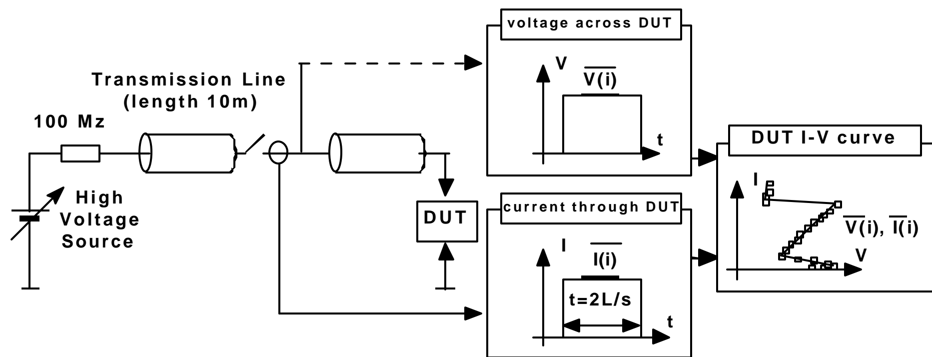
Second, DC measurements are limited because they typically do no reflect the faster rise and fall times of ESD stress pulses. For example:

- Any bipolar resistor does have a characteristic time constant (base transit time) that reflects its speed of operation. A silicon-controlled rectifier needs two such time constants to fully reach its desired ESD operation mode (latch). For devices processed in advanced silicon technologies these time constants are well within the range of ESD current rise and fall times. Therefore one cannot evaluate the physical behavior for ESD conditions with (infinitely) slower DC measurements. Therefore DC measurements may actually hide (too) slow a behavior of protection devices under ESD. [5-6].
- Semiconductor junctions and the dielectric materials in advanced technologies form capacitors, respectively capacitor dielectrics that will carry significant current under fast transients (I = C dV/dt). These currents that do influence the physical behavior under ESD stress conditions are not generated with the much slower DC measurements [7-8]. Transient currents maybe beneficial or not for the operation and definition of the ESD discharge path. Therefore, DC measurements can give a skewed view of the ESD behavior since the transient currents are not present.

TLP characterization

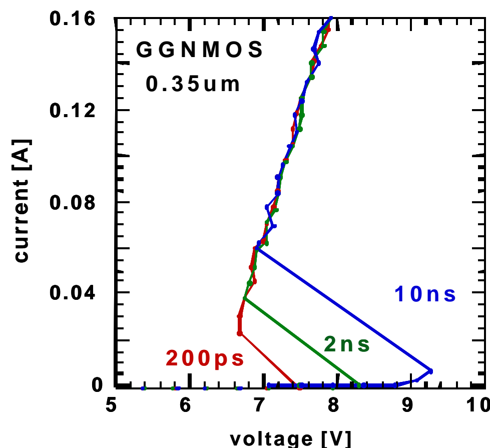
It is obvious that one needs to characterize the silicon devices in the relevant current-domain and relevant time-domain. This can be done by fast square pulse testing, better known as Transmission Line Pulsing (TLP) since it was first introduced for ESD design by Tim Maloney in 1984-85 [9-13].

In a TLP measurement one typically applies a short (100ns wide) and fast (few nanosecond rise time) current pulse to a device-under-test. The device response (current vs. time I-t and voltage vs. time V-t) is measured by an oscilloscope. From the recording one will extract one data point of the current vs. voltage curve (I-V). By re-doing the experiment with a different amplitude current pulse, one will measure more data points of the I-V curve.



Typical TLP test system measurement set-up.

Again referring to the Wunsch-Bell curve, it is obvious that by using the short duration pulse, one will be able to test with higher current levels that are typical of ESD stress events (several Amperes).



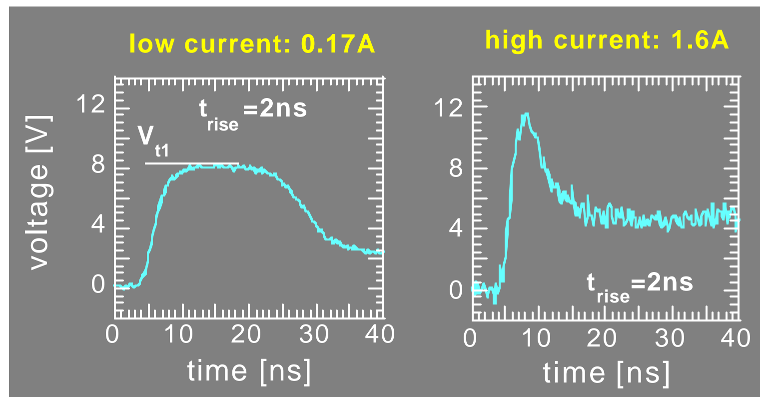
Rise time variation experiment of a gate grounded NMOS (0.35um CMOS)

Moreover, given the fast rise and fall times, the TLP techniques should give us a better understanding of the dynamic effects such as trigger speeds and transient currents

under ESD type conditions. The trigger speed of a device can be very well analyzed from the TLP V-t response. However, a warning should be issued that the exact rise time of the TLP curve is very important for the outcome of the measurement. ESD events such as HBM and MM are modeled (and thus tested for) with 10-20 ns rise times. Several authors have shown significant changes in TLP I-V behavior for rise times varying between 200 ps and 20 ns. Miscorrelation between HBM and TLP results has been reported [14-15]. They can typically be traced back to rise time differences in the applied TLP and HBM test methods. A significant pitfall comes from the fact that in most TLP set-ups the I-t and V-t response from one measurement is reduced to a single data-point. As such trigger overshoots or trigger delays may be masked or hidden from the TLP I-V curve. [6,11].

In advanced silicon technologies, the TLP data and measurement technique are invaluable. The intrinsic sensitivity of the circuit nodes that must be protected is continuously increasing and has arrived at extremely low levels. In the most advanced 0.10um and nanometer CMOS technologies designers are faced with gate oxides not thicker than 2-3 nm. Such gates fail when 5-7 Volts is applied under ESD stress conditions. This means that their design window is extremely narrow: they need to fit a 2-3 Ampere ESD pulse within a window of maybe 2-3 Volts. In the best case, that leaves about 1.5 Ohm of dynamic on resistance for the ESD discharge path.

Although it would be desirable, there is no direct application of TLP, even Ultra-Fast TLP, for CDM characterization of IC protection circuits. As described by Gieser [16-18], the fundamental difference between CDM and TLP is that CDM is a one-pin test, while TLP requires the selection of two IC pins. Therefore, the ESD discharge path for both CDM and TLP will differ within an IC. If the stress path is different, there will be by definition, no correlation possible between the test results. Nevertheless, fast TLP offers opportunities to the engineer to deduce CDM relevant parameters of the ESD protection design, such as the transient voltage response.



Transient voltage analysis of the triggering of an ESD protection clamp (0.13um CMOS)

For the actual protection device analysis, the transient voltage overshoots before the protection device clamps will determine the reliability of the input gate oxide under both CDM and HBM/MM type stress. Therefore, the characterization of the silicon must include transient voltage analysis of the protection device trigger (see Figure above) [6].

This can be done with a TLP test system that can resolve clearly defined rise times and measure the voltage response accurately during the first few nanoseconds of the

protection operation. That time interval is typically ignored in many TLP measurement set-ups.

The actual measurement of the voltage transients during triggering is unfortunately rather complicated. We measure a device with variable impedance: from infinity before triggering, to almost zero after triggering, while going through a negative resistance phase. As such, the measurement event goes from a voltage-forcing mode to a current forcing mode. This means that calibration (with a constant load, e.g. 0 Ohm or 50 Ohm) becomes very difficult as parasitic inductive effects, which change as a function of current during the measurements, and must be removed from the data.

A practical approach to assess this ESD protection problem is to measure the response of a protection device in parallel with a thin gate oxide monitor [6]. Then at least one can determine whether or not the protection device was triggered sufficiently fast, even if the measurement of the exact voltage transient may not be fully accurate.

For advanced IC technologies, one can add that IC dies become increasingly bigger (more functions are integrated) and that the speed requirements are ever faster and faster. The latter limits the designer in the silicon area (read: parasitic capacitance) that can be added to provide ESD protection. Smaller devices will have higher on-resistance… It is clear that the design space is disappearing, and TLP characterization becomes an absolute necessity to explore that ever-narrower design space.

There simply is no margin left for sandbagging the design. Therefore one must obtain a very accurate characterization of the silicon devices for their ESD applications. This can only be done through accurate TLP testing.

Moreover, the cost of one re-design for ESD far exceeds the cost of a TLP system: over one million US dollar for a complete mask set in sub-0.10um CMOS compared to a few ten thousand to some hundred thousand US dollars for a home or commercial built system. Thus, the challenges to ESD characterization must be addressed with further development of the techniques described in this manuscript before it can be effectively applied for ESD protection design.

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Chapter 8

Device and Technology Effects

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Introduction

For the semiconductor devices the process technology plays a major role in determining the impact on the device performance under ESD conditions and this in turn on the strategy for the protection circuit design. In this section we will consider the history of the process influence, the ever-changing impact of the technology development, and the challenges as we move forward to sub-0.1 um technologies.

Early Protection Designs

The sensitivity of ESD protection design to the electronic technologies is well known. In the late 70's the protection devices for the integrated circuit (IC) chips consisted of a substrate diode whether it was intentional or naturally formed as a parasitic diode for any signal pad that is connected to a diffusion of the opposite polarity from the substrate. Subsequently in later years systematic protection designs were investigated in order to improve the efficiency of the protection circuits and their compatibility to the function of the signal pin. Next, dual diode clamps to both power supplies, Zener diodes, and transistor configurations were used for MOS technologies, and the bipolar NPN for the bipolar technologies. The optimization of the protection schemes and their effective design for protection of the input buffer gate oxide was not all thoroughly understood and this led to a lot of trial and error protection designs. There have been many advances in the protection designs and a summary and the challenges are given in the section on ESD Protection Design of this paper.

Systematic Studies

By the mid-80's, with more systematic research work by several new ESD technologists at both industry and universities from U.S., Europe, and Japan, novel protection devices started to appear. The novelty involved characterization of the protection circuits, their parameter variations for improved design, and their implementation on the IC chip with effective layout. It was soon to be found that the layout is the most critical for protection design operation to avoid current crowding effects.

The improvements in the device designs and layout methods rapidly progressed by the later part of the 80's. The new protection devices included first field oxide device formed with minimum diffusion-to-diffusion spacing as parasitic NPN devices that effectively conducted the ESD current as a bipolar device. This later extended to NMOS transistors

with the same principal. With the MOSFET it was recognized that under ESD the device forms as a parasitic bipolar npn with the Drain as the Collector, Substrate as the Base, and the Source as the Emitter. This understanding was critical since this parasitic device formed the workhorse to conduct at least 5X current density compared to the normal surface conduction of a MOSFET during circuit operation. The efficiency of this approach however hinged on improved layout methods. The critical layouts involved the placement of contacts from the diffusion edge for field oxide devices and from the gate edge for the NMOS transistors. Other novel protection devices as the Silicon Controlled Rectifier (SCR) were introduced to revolutionize the protection design concept.

Device Physics

The NMOS transistor represents the high current behavior under ESD conditions as shown in Fig. 1a. During ESD transient stress pulse the drain junction goes into avalanche generating substrate current and the subsequent voltage drop from the substrate current flow causes forward bias of the source substrate junction which eventually results in a parasitic bipolar npn, as shown in Fig. 1b. This npn conduction is efficient for ESD and can be 10X in current density compared to the surface conduction of a MOSFET. Typical values of 5 mA/um as characterized with 200 ns pulses to represent the ESD event are considered to be the desirable goal for ESD requirements.

Impact of Advanced Technologies

With a deeper understanding of the intentional protection design such as using the bulk NPN conduction of a MOSFET or the anode-to-cathode conduction of an SCR in CMOS technologies, much improved ESD performance was achieved. The scaling of the technologies for improved IC chip performance and the introduction of other novel process technology features for the other reliability considerations eventually led to the degradation of the ESD performance that was built up on during previous 10 years from late 1970's to late 1980's. Therefore this again led to more research work and methods to overcome the technology effects. The cross-section of an advanced NMOS transistor is shown in Fig. 2.

The main technology effects are:

- **Lightly Doped Drain (LDD) junctions for Channel Hot Carrier reliability**
- **Surface implants to control punch-through effects**
- **Pocket implants for threshold control**
- **Low substrate resistance materials for improved Latchup reliability**
- **Shallow junctions for improved transistor performance**
- **Scaling of minimum channel length for high performance**
- **Silicided diffusions and gates for low resistance and high performance**
- **Ultra thin gate oxides for high speed circuit designs**

As these advances are made in the CMOS technologies all of them have had serious negative impact on ESD designs. In most cases the transistor advances were made with no consideration to ESD robustness. There are a number of papers published during the last 12-15 years that gave much insight into the parasitic bipolar conduction and the reduction in the transistor's ESD robustness (measured in terms of the failure current It2 [1]) with scaling. Also, many have used simulations to understand the heating

effects. Each of the major process impact parameters is considered here to understand the nature of the impact.

1. Graded Junctions

The drain engineering to grade the junctions and thereby reduce the peak electric field to improve the hot carrier reliability started in the mid-80s. There are different methods to do this but the popular way is shown in Fig.2 where shallow n- regions are introduced. With the LDD the avalanche multiplication efficiency is reduced and has a direct impact on the generation current (Igen) required to sustain the lateral npn. This means a higher holding voltage and higher power dissipation, and hence subsequently lower It2. For all the near future technologies some form of LDD structure is going to be important for hot carrier reliability even with the scaling of the operating voltages. Therefore for the next generation a more clear understanding of the LDD effect, the variations with the energy and dose of the implants, and the process optimization for both hot carriers and ESD reliabilities is needed. Much research work can be done with this effect alone but only with the help of very predictable simulators.

2. Drain and Channel Engineering

As the technologies scaled towards the deep submicron channel engineering to control the transistor Vt or the off-state leakage has seen progress. These issues will become critical for the continued scaling of the application voltage. The pocket implant shown in Fig. 2 is now an essential part of the advanced transistor and has been seen to reduce the It2. Therefore this again points the need to understand and predict the impact on ESD reliability as more and more necessary changes are explored for the transistor performance and reliability.

3. Channel Dimensions

The gate length or the effective channel length determines the beta of the lateral npn that is critical for It2. The trend has been that as the channel length is scaled down the beta increases and has a favorable effect for ESD. Even this is now showing signs of anomalous and unexpected behavior where for the sub-0.3 um transistors, the It2 has a reverse trend with length. It is not yet known whether this is related to localized heating with reduced volume of the shallow channel region near the drain. Similar to the length effect the channel width is also showing some current crowing effects. This is again a critical area for understanding using simulations. Further, as the feature lengths are reduced the PMOS transistors are starting to play an unexpected active role and

4. Silicide Effects

The introduction of silicides had about the largest detrimental effect on the ESD performance of the transistor. The presence of silicide on the diffusions drastically reduces the ballast resistance and leads to current crowding. Although there have been excellent studies to understand the device phenomenon with silicides, the optimization with predictive capability has not been achieved especially with respect to the silicide process conditions.

5. Gate Oxide

The gate oxides have always been a concern for ESD but most of the reliability has been achieved with proper clamps. However, with the scaling towards ultra thin gate oxides is causing serious concern for both thermal damage as well as latent damage from the transients of the ESD pulse even with the presence of a clamp. The anomalous length effect mentioned above could be related to the thinner gate oxide effect that needs further investigation with sophisticated thermal modeling.

6. Substrate Effects

It is now well recognized that the effective substrate resistance, which is determined by the thickness and doping of the Epi layer as well as the p-well shown in Fig. 2, can have a strong influence on the ESD robustness of the transistor. Likewise, in a PMOS transistor the nwell resistance has effect on the ESD designs using lateral diodes or SCR's. There are now numerous complex pwell process considerations for the next generation of technologies that will surely present more challenges. Another consideration is the trend towards Silicon-on-Insulator or SOI. In SOI the isolation of the substrate essentially eliminates the heat sink and causes reduced ESD efficiency. There are some thermal modeling efforts in progress but the full implications with advanced SOI with very thin insulating buried oxide are still unknown.

Conclusions

As we have seen, the CMOS technologies used in the mainstream IC designs are posing a high uncertainty in the capability for ESD design. In addition, the increased use of Bipolar-CMOS for high voltage applications, GaAs for optical communications, and other new trends such as Si-Ge processes for RF applications are sure to cause more limitations on the ESD reliability. These future trends are dealt with in more detail in a different section of this white paper.

There have been numerous publications that present good insight into the device physics of the technology advances and the impact on ESD. These are listed in the bibliography.

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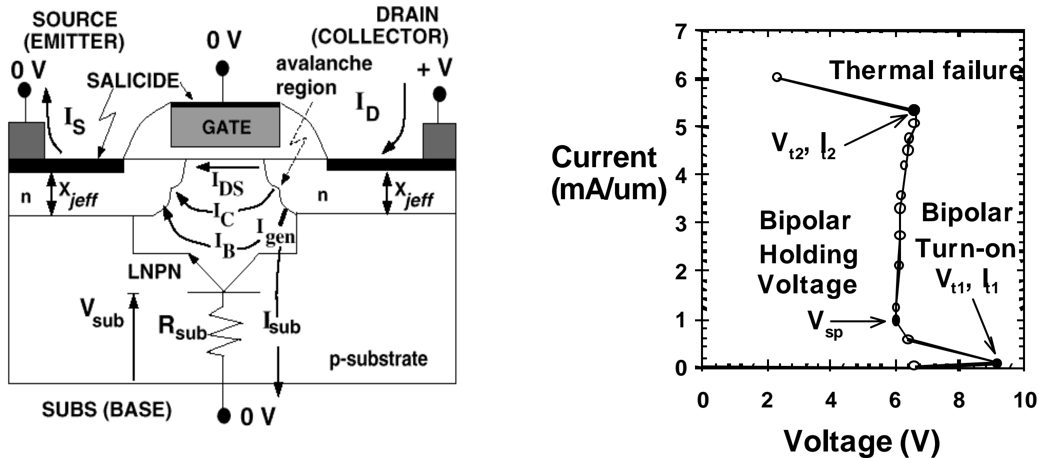

Fig. 1. The cross-section of an NMOS transistor showing the parasitic bipolar npn in (a) and the IV curves showing the trigger of this device in (b). Note that the efficiency of this device depends on the avalanche injection at the drain junction, which in turn is determined by the channel length, the junction depth and the drain engineering that is done to improve the transistor performance and overall reliability. From the IV curves it can be seen that the thermal breakdown (It2) is the indicator for ESD performance and is again determined by the process device parameters.

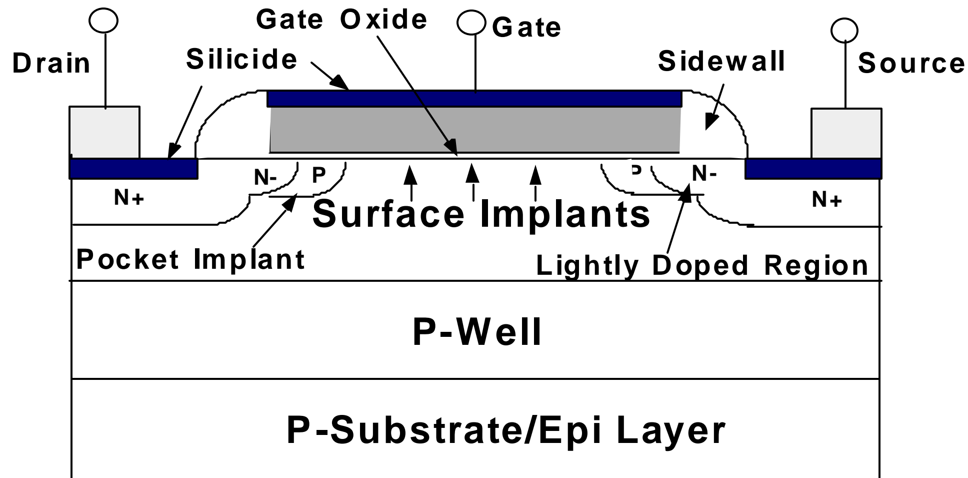

Fig. 2. The cross-section of an advanced NMOS transistor showing the main features that include the silicided diffusions and gate, the sidewall oxide to allow the shallow N-regions for electric field grading at the drain/source junctions, the P pocket regions for reduced leakage, the surface implants for the transistor threshold control, and the pwell and Epi layers for high performance substrates.

Chapter 9

Protection Design

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Introduction

Advancing technology gives us new electronic products every year, often with the most aggressive process technologies quickly moving into high-volume manufacturing. These become our latest personal computers, enterprise servers, telecommunications products, etc. The competitive environment requires high reliability and quick development of high-yield manufacturing, and of course ESD protection is an important part of this. New (or newly scaled) semiconductor processes and products face a set of ESD protection challenges as they are developed. Some are familiar and relatively easy to solve, others are more difficult. Some have wide applicability; others are narrow in scope, perhaps unique to a particular product or application. The semiconductor technology itself is the starting point for the ESD design environment, and that environment is a changing one. Designers make adjustments to accommodate ESD protection, but rarely compromise product performance. At times, the technology provides new opportunities for ESD protection, as we will see later in this section.

The aim of this section is to summarize the familiar challenges facing protection designers of electronic products. These are usually integrated circuits, semiconductor devices, or devices employing semiconductor technology and handled similarly in manufacturing and use. When those challenges are recognized and addressed with a look toward the future, good ESD-related research work can result. We hope to inspire good research programs with this overview of ESD protection design.

You will find a tremendous amount of technical literature about ESD protection design, including review articles, which will detail the state of the art regarding many of the topics below. Other references on this ESDA.org web site will supply an appropriate bibliography. This article finds its worth in being an overview that intends to point out the research opportunities as we move forward.

Scope

Silicon CMOS technology accounts for the largest volume, in number of wafers and dollars, of product in today's electronics industry. Accordingly, it is our best model for scrutiny of ESD protection design; other technologies take their cue from it and try to apply the same methods if possible. We'll address the various elements of ESD protection design for bulk CMOS, and then make some brief comments concerning other semiconductor devices.

All treatments of ESD protection design aim at good performance under the various standards for ESD evaluation, most notably the Human Body Model and the Charged Device Model. The Machine Model can also be important. These test standards are described elsewhere on this ESDA.org web site.

In the end, the semiconductor component is integrated into some kind of final product, generally known as the system. Systems are also ESD checked under a different test regime, but solving problems involves the interaction of component-level and system-level ESD protection. Component self-protection in the context of systems is also a topic of interest, and we will touch on it at the end of this section.

We'll start by dividing ESD protection for a semiconductor chip into local protection (local to the pin under test) and global protection (applying to the whole chip or entire ESD current path, including power supplies and metal connections). Each of the elements in these categories has been the subject of significant research.

Local Protection

CMOS IC pins are most often inputs, outputs or some combination of these (called an I/O) if they are not power or ground pins. Each of the major aspects of local input and output protection has been the subject of extensive research work.

Diodes

For a typical input-only pin, the preferred protection scheme is the dual diode, which by the means of two diodes routes the ESD current either to the power supply (call it Vcc) or to ground (Vss). In order to use dual diodes in their simplest form, it must be acceptable during operation for voltages to be confined to the Vss<Vin<Vcc range, although there are methods (still using diodes) to tolerate mixed voltages. Usually there is "secondary protection", involving a series resistor and more diodes, to further protect the input buffer from damage.

Contemporary research on these diodes has included the effects of scaling and trench isolation on their series resistance and performance. There are methods to block the trench isolation (as with poly gates) in order to reduce series resistance. With higher frequency designs, diode capacitance and RC delays through both the primary and secondary protection are of growing importance. These high frequency considerations open up substantial new research opportunities.

Outputs, I/O, and FETs

CMOS outputs and I/Os usually involve a large inverter to drive the pad and line, with PMOS FET pullup and NMOS FET pulldown. As process scaling takes place and signal lines remain around 50 ohms impedance, the transistors get smaller and may need to be augmented by dual diodes in parallel. This is another important contemporary research subject, involving more tradeoffs of capacitance, ESD protection, and RC delay. SCRs may also be in parallel with outputs, see below.

Outputs also can have special circuitry to make them voltage-tolerant, or drive high voltages with thin gate oxides. They may be made with thicker, high-voltage gate oxides

in a dual-oxide process. All these methods are of interest to researchers, as are other methods intended to enhance ESD performance through circuit and device design.

The NMOS output device (and the related grounded-gate NMOS protection device) has been of great interest to researchers and has inspired many papers. Controlling npn snapback (the breakdown mechanism of NMOS FETs) through ballast resistance in the NMOS drain, tailoring the epi or substrate, and other means, continues to be a popular subject of research work. Snapback can be destructive, or non-destructive, depending on how the snapback event is engineered, so many of these efforts focus on how to engineer the event so that it is non-destructive. Consider the following haiku:

Spill some electrons
From source to substrate to drain
Smoothly, to protect.

This can be seen as the theme of many a research paper about ESD and snapback in NMOS devices. Curiously, the NMOS output FET is rarely the only path for ESD current. Even when the NMOS is an open-drain device with an external pullup, it can usually be accompanied by a diode to Vcc, to take the pressure off the NMOS pulldown device in snapback. Nonetheless, snapback engineering of the NMOS device will continue to be an important research subject.

PMOS devices also appear in outputs, of course, and are of concern in the ESD event. Because electrons and holes have different ionization rates, the breakdown event is different and there is no distinct snapback event with negative differential resistance, and its accompanying tendency to focus current and cause local destruction. Nonetheless, with device scaling and device engineering for performance, there are hazards and failures in the PMOS device as well. These are being studied and reported by researchers with increasing frequency, but we need more insights into PMOS behavior in scaled processes.

SCRs

The pnpn device introduced by Shockley has always been a part of CMOS technology because it resides intrinsically in any CMOS IC fabricated on bulk or epitaxial substrates. This structure is commonly called the SCR (for silicon-controlled rectifier, or semiconductor-controlled rectifier) and is best thought of as two merged transistors, a pnp and an npn, which can latch into a high-current, low-voltage state if they are both turned on. But CMOS technologists always devise rules to inhibit accidental triggering of CMOS latchup between Vcc and Vss in the integrated circuit. SCRs can be designed to allow local protection, because an SCR can clamp much ESD current non-destructively.

Much contemporary research has been devoted to SCRs for protection of inputs and outputs. Triggering the device for ESD, without interfering with IC operation, is a major goal and source of innovation. Gate oxides, masking options and even process adjustments can become involved in the solution. The thickness and resistivity of the epitaxial layer, if any, plays a major role. But a successful SCR protection scheme can accomplish a lot in a small area if it works well. For example, voltages higher than Vcc can often be tolerated in mixed-voltage applications by using an SCR protection device. In this way the SCR replaces dual diodes for input protection. The SCR has also been employed parallel to output devices as a low capacitance current shunt.

Because of their 2-transistor, pnpn structure, SCRs trigger more slowly than some other protection devices. For that reason, it is important to characterize the devices for CDM performance as well as HBM, to assure that the final circuit also survives fast transients.

The SCR is best suited for bulk substrates, or substrates with thick or higher resistance p-epitaxy. At times, developers can get SCRs to trigger and work smoothly even with thin epi CMOS, but it is more difficult and usually requires close cooperation with process engineers and transistor developers. Such conditions are often unacceptable to companies planning process and product development for high-volume manufacturing (HVM), and they will avoid SCRs in favor of other design methods. This critical aspect of SCRs is often unmentioned in reports of SCR protection devices for ESD.

Global Protection

Power Supply Clamps

ESD currents must find their way through the chip nondestructively. The local protection we described in the previous section is part of the solution, but not all of it. The ESD currents launched onto power buses (or originating from them, as in the case of the CDM) must also be nondestructive. To guarantee this, local protection must be complemented by power supply protection, to assure that internal circuitry not be the weak point in the ESD path.

Among the variety of power supply clamps reported, the most popular to date have been some kind of large NMOS or PMOS device, set up to clamp Vcc to Vss on a temporary basis. Moore's Law has been of benefit here, because MOSFETs can sink more and more current per unit area as devices scale; indeed the pulsed current goes inversely as the square of the minimum device dimensions. At the same time, ESD events are about the same as always (amps and nanoseconds), meaning that protection can be achieved in smaller and smaller area. As scaling continues, the somewhat larger current per unit area available from NMOS devices, as compared with PMOS, becomes less and less meaningful because a supply can be well protected within the space occupied by a single bond pad. This author far prefers PMOS devices for supply protection because they avoid the hazards of NMOS snapback, and work well in stand-alone mode (as is nearly the case with small power supplies, where clamps are needed most) even for CDM events.

Power supply clamps are now used on billions of dollars worth of product but there are still numerous opportunities for fundamental research. For example, we don't know the thermal limits as we keep scaling the MOSFET dimensions and pack the pulsed ESD energy into a smaller area. At what level will local thermal runaway and filamentation occur? Related to this is determining a "safe" pulsed overvoltage level for the Vcc power supply. It is well known that short-term (nanosecond to hundreds of nanoseconds) overvoltages will not cause damage to the power supply, while longer term or dc overvoltages will cause failure. For a given technology, how does this time-voltage tradeoff go? And what is the trend with technology scaling? Many believe the answer is related to gate oxide wearout and some research has been presented, but further work is welcome.

Other power supply clamps have included bipolar devices (popular for a while on CMOS processes, but now mostly obsolete due to process scaling) and some breakdown-

related devices. SCRs have been proposed but have largely been avoided because of the latchup hazard, i.e., the possibility of latching during burn-in or operation, thus destroying the component. A good test of proposed ideas in this area is to ask if the concept was successfully phased in on a product that was manufactured and shipped in considerable quantity—many ideas that work on a test pattern will not reach HVM.

Metallization

ESD current always has to pass through metal wiring on-chip. This takes place at the pins under test and usually also involves one or more power buses. Metal should not be allowed to conduct too much current per unit area, and should not add substantially to the series resistance in the ESD path. If it does add resistance, the protection level can be reduced and the current may find alternate "sneak paths". This is a particular danger on small power supplies. On larger supplies, the scaling down of voltage and higher circuit density has resulted in scaling up of current, so designs are less likely to include excessive series resistance on the power supply than has happened in the past.

Aluminum and its alloys were, for a long time, the standard integrated circuit metallization. The industry is now well on the transition path to copper metal. This has the beneficial effect on ESD of being able to pass more cross-sectional pulsed current through the metal, with attendant changes in design rules. Most of these effects have been worked out and published, but there are still some opportunities relating to metallization. The issue of latent damage to the metal (due to electromigration, or EM) caused by otherwise non-destructive ESD pulses was pretty well studied for aluminum, but has not been very well studied yet for copper. Even the aluminum studies were mostly wafer-level stressing; we could use some traditional EM oven studies following ESD stress.

Another opportunity relates to low-k dielectrics. At present most of these might be called "lower-k" dielectrics because they retain most of the properties of silicon dioxide, including high-temperature processing. But some proposed low-k dielectrics, with much lower k and lower temperature processing (400C for example), would provide an interesting ESD study. As one can heat copper to over 1000C without melting it, one can conceive of ESD pulses that are non-destructive to the metal that may cause damage to the dielectric, on account of being too hot. The question is how hot for how long will cause dielectric damage: what is the time-temperature tradeoff. This has not yet been studied for aggressive low-k dielectrics.

Simulation

Global protection includes putting together designs with automated tools. Some research studies have looked at this but so far they have met with mixed results. The concepts to be checked are clear enough, but it is difficult to utilize a company's design environment and product database to check, automatically, all rules relating to placement of ESD protection. Even if automated checking solutions are devised for one product or group of products, the fault coverage is not 100%, and the system may be hard to adapt to other products in the same company. Workers are encouraged to continue these studies and report them at conferences, but are also encouraged to provide their own "reality check" before the audience does.

Protecting Other Semiconductor Devices

Other semiconductor devices can and do benefit from the basic principles of ESD protection, as largely developed by the silicon CMOS integrated circuit industry. Examples of other electronic devices needing ESD protection include
Silicon on Insulator (SOI)
Optical devices, e.g., LEDs and lasers (mostly III-V semiconductors)
RF CMOS ICs
GaAs FETs, GaAs and other high-speed III-V ICs
Magnetoresistive (MR) heads (for disk drives)
SiGe bipolar ICs
MEMS (microelectromechanical systems)

All of these need ESD protection, and all have been the subject of research efforts. MR heads have been included as electronic, not really semiconductor, devices because they are so ESD sensitive. They are also important to the further development of computers and semiconductors and need to be produced in high volume. In all of these cases, we start with the basic HBM and CDM ESD component tests and apply whatever methods we can to shunt the current to ground safely.

To solve these more unusual problems, it will be necessary to think "out of the box" at times. Sometimes an old method will find a new application. For example, spark gaps (which were largely unsuccessful on ICs in their early attempts, 30 years ago) may be used in MEMS devices.

Conclusion

ESD protection of electronic devices continues to provide challenges for the designer. But, even in a research context, ESD protection cannot be considered by itself. ESD protection must be consistent with the operational and performance goals of the product as well. In other words, ESD protection must contribute to the product and not interfere with delivering a competitive product. As we evaluate the various approaches and solutions to ESD product, we should ask if the methods under consideration are suitable for a real, marketable product. Could we manufacture and sell a million of them? Is this kind of manufacturing underway, and successful? Answers to such questions, even if only on paper, can discover pitfalls and also validate new ESD protection approaches.

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Following is a short list of books and review articles about ESD protection. These works cite numerous references and help the reader to access most of the literature on ESD protection.

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2. A. Amerasekera and C. Duvvury, *ESD In Silicon Integrated Circuits*, 2nd Edition Wiley (London), 2002, 412 pages.
3. T.J. Maloney, "Designing Power Supply Clamps for Electrostatic Discharge Protection of Integrated Circuits", Microelectronics Reliability Vol. 38, No. 11, pp. 1691-1703 (November, 1998). This journal issue also has other review articles about ESD protection.
4. S. Dabral and T.J. Maloney, *Basic ESD and I/O Design*, published by Wiley Interscience, November 1998, 302 pages. Book listing can be seen at http://www.amazon.com/exec/obidos/ASIN/0471253596/

Chapter 10

Future Issues

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In the future, there are many challenges to both the present technologies and new fields in the area of electrostatic discharge protection.

CMOS Technology

In CMOS technology, the nano-structure age has begun where the silicon MOSFET transistor channel lengths are decreasing below 100 nanometers. MOSFET transistors dimensions are scaled according to MOSFET constant electric field scaling theory. MOSFET constant electric field scaling theory scales the dimensions of the transistor to maintain the same electric field across the oxide film. MOSFET scaling has reduced the oxide thickness from 1000 A thickness to less than 20 A gate in recent generations. With oxide scaling, the gate dielectric breakdown voltage decreases. For reasons of dimensional similitude, the MOSFET channel length and other dimensions decrease. MOSFET channel length scaling decreases the MOSFET avalanche, and snapback triggering voltage. MOSFET scaling theory leads to higher doping concentration. As a result, the scaling of MOSFETs plays a profound role in the ESD robustness of the MOSFET transistor.

Scaling and the desire for improved performance has influenced both the silicon devices and wiring interconnect used in silicon technology. To improve the speed of high performance semiconductor chips, and to maintain dimensional similitude with the MOSFET transistor, interconnects are also scaled with the silicon devices and material changes continue to change. To achieve faster devices, interconnects have moved from aluminum-based to copper-based interconnect systems to reduce the resistance. To reduce the line-to-line and coupling capacitance, new inter-level dielectric (ILD) materials with lower dielectric constants have continued interest. ESD robustness of the wire interconnect and ILD dielectric are a strong function of the material melting temperature, stress characteristics, and dimensions. The material change, wiring hierarchy and architectures of the wire interconnects/dielectric system have significant influence on the ESD robustness of leading edge high-pin count advanced technologies.

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[2]. D. Lin, "ESD Sensitivity and VLSI technology trends: thermal breakdown and dielectric breakdown," EOS/ESD Symposium 1993.

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[11]. S. Voldman et al, “High Current Characterization of Dual Damascene Copper/Si02 and Low-K Interlevel Dielectrics for Advanced CMOS Semiconductor Technologies,” IRPS Symposium, pp. 144-153, 1999.

Silicon On Insulator (SOI)

To maintain performance objectives in CMOS, it is also possible to develop CMOS technology on insulators to lower capacitance. This can be achieved by using standard CMOS technology on a starting silicon-on-insulator (SOI) or silicon on sapphire (SOS) technologies. Many process technology techniques exist to form SOI wafers (e.g. SIMOX, SIBOND, “smart cut”) and SOS wafers. Continued development and research is needed in understanding the effects of ESD in SOI or SOS wafers. With the development of a mainstream SOI technology, SOI technology will be integrated with both copper interconnects, low k materials and features used in sub-100 nanometer CMOS technologies. As SOI MOSFET is scaled, the buried oxide (BOX) layer will also scale to reduce cost and improve thermal transport to the substrate material. With the thinning of the silicon film on the BOX layer, both partially depleted SOI (PD-SOI) and fully depleted SOI (FD-SOI) will become important. Although it has been demonstrated that good ESD results are achievable in PD-SOI, continued research and development is needed in the future for both PD- and FD-SOI devices.

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Low Power CMOS

CMOS can fulfill both performance and low power applications in today's marketplace. Low Power CMOS will be an increasing issue because of the interest in reducing power consumption and increased portability of electronic equipment. As a result, new research and design interest exists for achieving both low power CMOS design point of transistors and ESD robustness of the products.

Radio Frequency (RF) and GHz Technologies

With the growth of mobility and portability of today's society, radio frequency (RF) technology and Giga-Hertz (GHz) applications continue to grow at rapid pace. With the laptop, palm readers, cellular telephones, and the Internet, the wired and wireless marketplace will have a rapid growth in the next decade. High speed wired communications for 10 to 40 GHz Ethernet and SONET will fuel the need for RF technology. With the increased speed of these wired systems, the loading and RF quality of ESD protection strategies and components will have to be re-addressed. These wired systems will contain combinations of mixed signal chips, RF CMOS, Silicon-Germanium technology, Gallium Arsenide (GaAs), RF SOI and optical components. ESD will be a threat and a concern for high-speed circuitry in these technologies.

RF CMOS

ESD protection will be a concern in RF CMOS for applications above 2 GHz. To achieve high unity current gain cutoff frequencies in transistors, advanced CMOS technologies will needed to be used. This will require low capacitance and small MOSFET channel lengths. As a result, ESD devices will be smaller than standard CMOS technologies.

[16.] C. Richier et al, "Investigation on Different ESD Protection Strategies Devoted to 3.3 V RF Applications (2 GHz) in a 0.18 um CMOS process," EOS/ESD Symposium, pp. 251-259, 2000.

RF SOI

For radio frequency (RF) applications, ultra-thin SOI (UT-SOI) is used for high speed switches and other applications. Today, UT-SOI is scaling it film thickness to further reduce capacitance loading and improve its unity current gain cutoff frequencies. As the thin film SOI decreases its thickness, the thermal transport is altered because of the relationship of thermal bulk phonons and surface phonons. ESD research and development will be needed to evaluate RF SOI as it approaches its ultimate limits of film thickness.

[17.] J. Reedy and J. Cable, *RF and SOI Tutorial*, IEEE SOI Symposium, 1999.

Silicon-Germanium

Silicon Germanium technology will be a strong player in the GHz revolution for the next 10 to 20 years. Silicon Germanium transistors continue to achieve rapid increases in the transistor speeds pushing unity current gain cutoff frequencies from 1 to 100 GHz. The significant reason which is fueling the Silicon germanium revolution is that it can be integrated with CMOS technology in a standard foundry. Silicon Germanium applications consist of high speed oscilloscopes, cellular phones, GPS devices, and high speed wired communication systems. The understanding of SiGe ESD sensitivity will be of importance as these products have entered the mobile market. Even today, new devices such as SiGe:SiGeC hetero-junction bipolar transistors (HBT) are being explored to further extend the application space and transistor speeds.

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Germanium Heterojunction Bipolar Transistor with Carbon Incorporation," International Reliability Physics Symposium, 2002.

Gallium Arsenide

Gallium Arsenide has advantageous electrical and thermal characteristics (e.g. higher Johnson Limit) compared to Silicon Germanium devices allowing dominance in the power amplifier and other markets. GaAs will be a significant player in optical communication systems. GaAs lasers will also play a key role in these systems. Continued research and development in the area of ESD protection and the evaluation of GaAs process and device ESD robustness. As in SiGe technology, GaAs technology will be extended to GaInP and other Gallium compounds to produce more efficient and faster devices for the future.

[25.] U. Konig, "SiGe and GaAs as Competitive Technologies for RF Applications," BCTM, pp. 87-92, Minneapolis, MN, 1998.

Magnetic Recording Industry

Magneto-resistive (MR) Heads

Magneto-resistive (MR) read head is used in the hard drive disk industry for storage of information. The MR head senses a variation in a magnetic field from the disk as it sweeps over the disk. This signal is translated into a voltage due to the magneto-resistivity of the thin film magneto-resistive stripe on the TiC wafer. The areal density of information on the disk continues to increase forcing the size of the MR stripe to scale with each disk drive improvement. The ESD (HBM) sensitivity of a typical MR head is 150V. These thin film stripes do not have ESD protection solutions because of the physical size of the MR head, cost, and they cannot be built on the wafer due to the lack of a silicon wafer. ESD protection of MR heads is a continued area of research and growth in MR stripe itself, the armature, head gimbal assembly and other components of the disk drive system. Areas of research consist of understanding of magnetic phenomenon, thermal physics, magneto-thermal research, electrostatics, design characterstics, failure analysis, and failure mechanisms.

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Giant Magneto-resistive (GMR) Heads

Giant magneto-resistors (GMR) heads are devices that follow the MR head designs to improve signal improvement with the decreased areal density of the disk. GMR devices utilize a spin valve (SV) for initialization of the GMR head. GMR heads are scaled in comparison of MR heads leading to an increased ESD sensitivity (e.g. 30 V). GMR

heads experience “spin valve reversal” as a result of the ESD event, causing de-initialization of the magnetic dipole alignment. This is followed by MR melt damage at higher currents. Research, design and understanding of the ESD sensitivities of GMR devices from EOS, ESD and EMI are ongoing today.

Tunneling Magneto-resistive (TMR) Heads

Tunneling MR (TMR) head are the next generation that utilizes multiple control layers allowing the quantum tunneling of current through a thin film in a transverse fashion. ESD sensitivities of TMR heads have been shown to be below 10 V HBM protection levels. Significant research will be needed to evaluate the feasibility of manufacturing and ESD protection of these elements. Additional to this device, there are a significant number of alternative MR heads for the future.

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Photolithography, Masks, Reticles and Pelicles

Photolithographic masks used for construction of semiconductor chips are key to the ability to continue scaling of technology to smaller dimensions. Recent studies show that shapes on masks have undergone ESD charging and discharging to adjacent shapes causing damage to the masks. The control of static charge on lithographic tooling equipment, and masks will be of significant importance for the semiconductor industry. Research in understanding the discharge effects, mask damage, and defects as well as development of new inventions, materials and solutions will be needed in the future as the mask dimensions continue to be decreased.

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MEMs

The subject of microelectronic machines, known as MEMs, is a growing field of microelectronics that has ramifications from electro-mechanical devices, such as accelerometers, to biomedical industry. The ESD sensitivity of MEMS will be an area of significant growth as the MEMs interface with real world environments where static charge is present. Today, there has been little focus on the ESD sensitivity of MEM devices. At the present time, few publications in the literature on the ESD protection or sensitivity of these devices exist today. As MEMs grow as an important part of society, the ESD sensitivity of these machines will become more important for their functionality and safe operation.

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